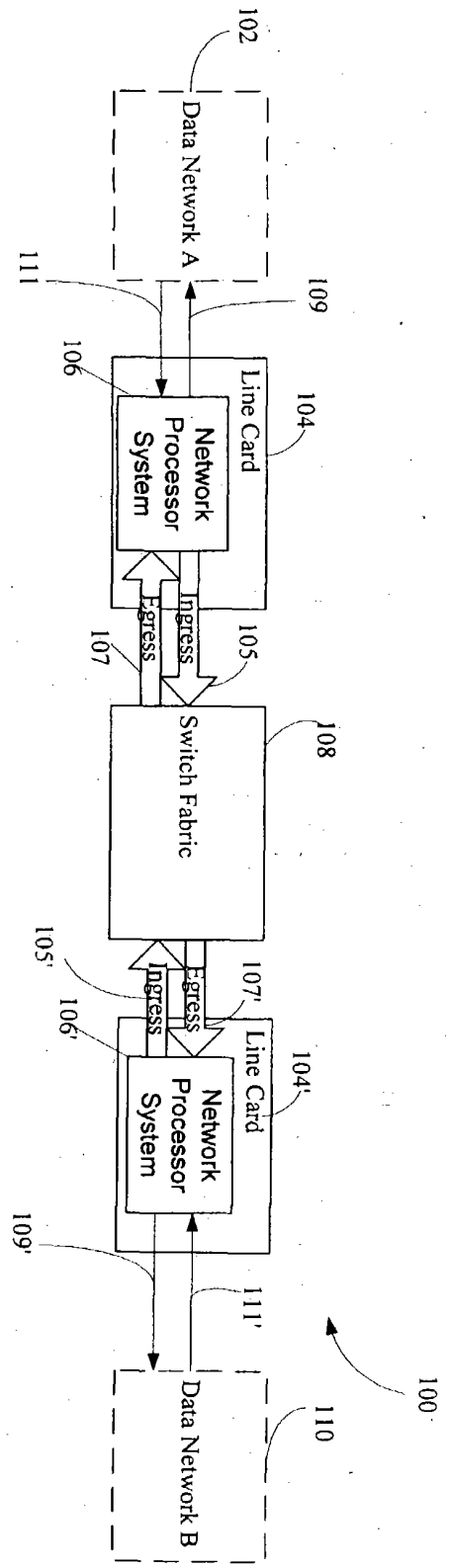

102
Data Network A
111
109
106
Line Card
104
Network Processor System
Egress
Ingress
107
105
Switch Fabric
108
105'
Ingress
Egress
107'
106'
Line Card
104'
Network Processor System
109'
111'
100
110
Data Network B

FIG. 1

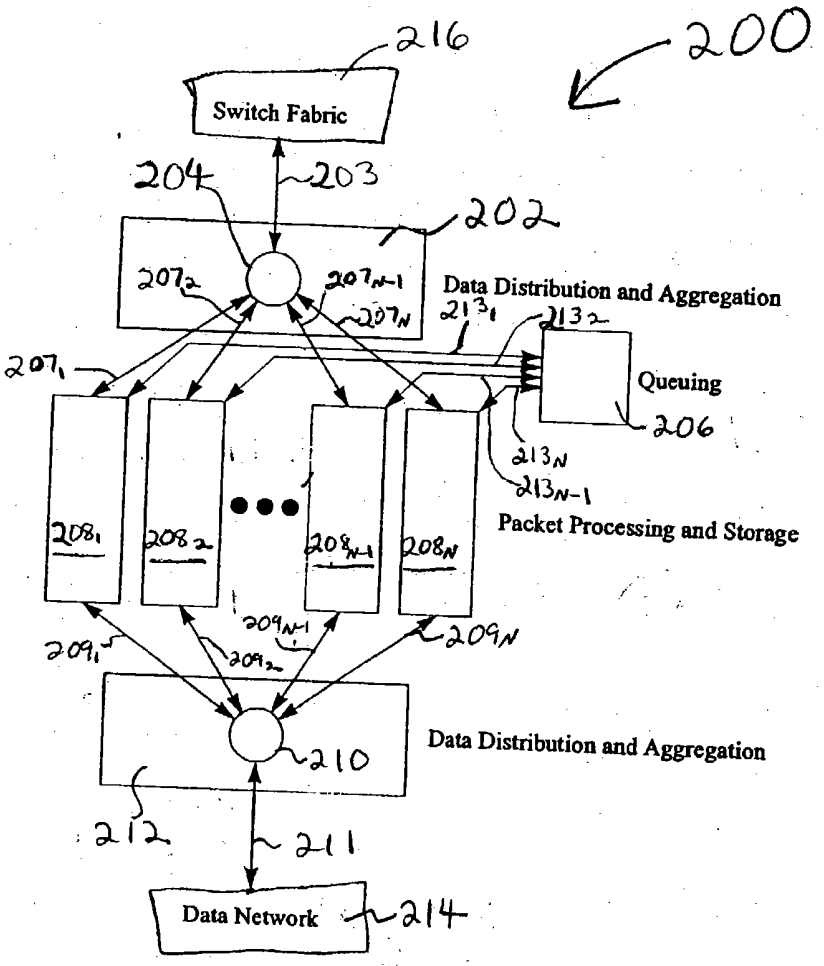

200
216
Switch Fabric
204
203
202
207_2
207_{N-1}
207_N
Data Distribution and Aggregation
213_1
213_2
207_1
Queuing
206
213_N
213_{N-1}
Packet Processing and Storage
208_1
208_2
208_{N-1}
208_N
209_{N-1}
209_1
209_2
209_N
210
Data Distribution and Aggregation
212
211
Data Network
214

FIG. 2

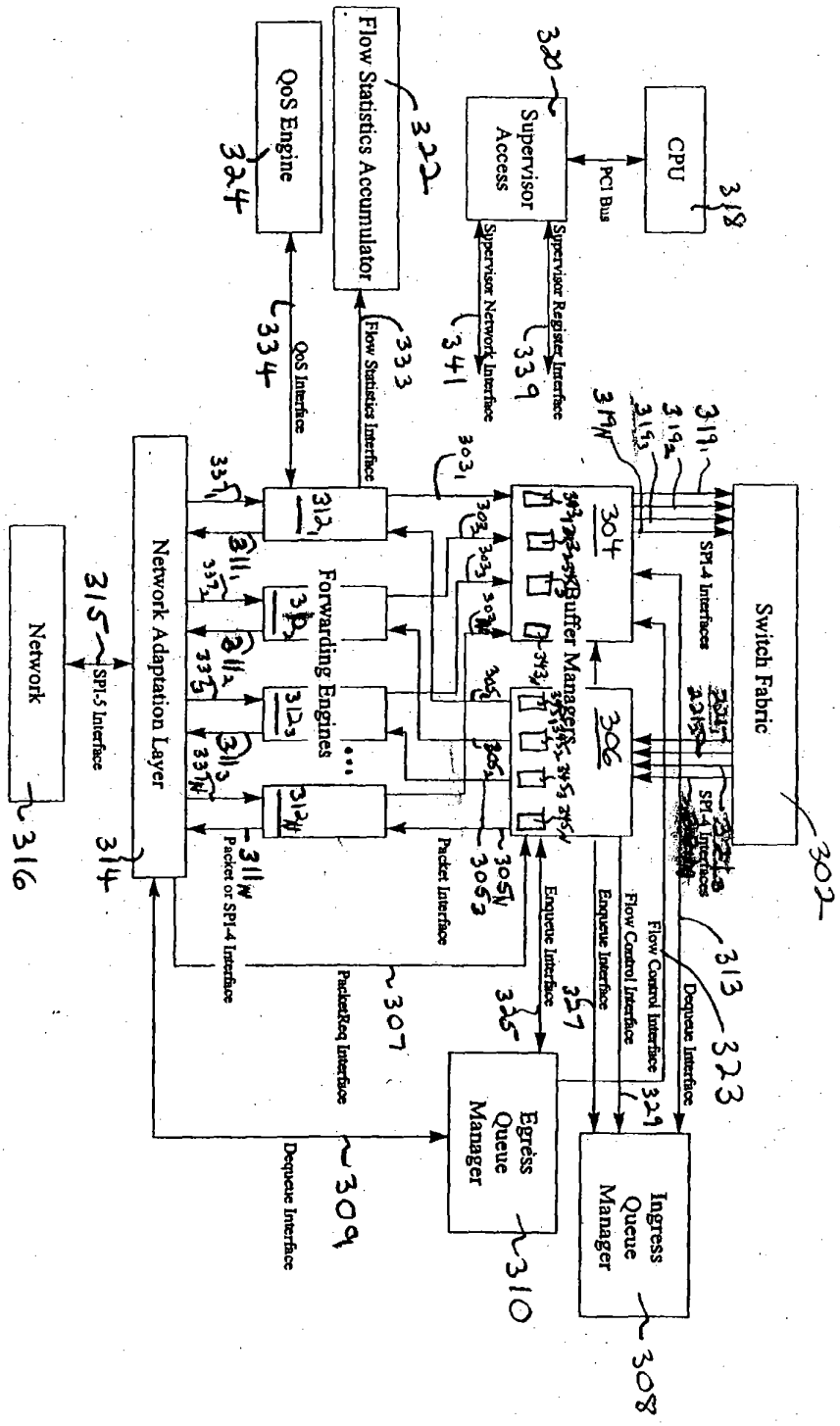

CPU
318
Supervisor Access
320
PCI Bus
Supervisor Register Interface
339
Supervisor Network Interface
341
Flow Statistics Accumulator
322
Flow Statistics Interface
333
QoS Engine
324
QoS Interface
334
Switch Fabric
302
SPI-4 Interfaces
Dequeue Interface
323
Flow Control Interface
Enqueue Interface
325
327
Buffer Manager
304
306
Ingress Queue Manager
308
Egress Queue Manager
310
Packet Interface
PacketReq Interface
307
309
Forwarding Engines
312
Network Adaptation Layer
314
SPI-5 Interface
315
Network
316
Packet or SPI-4 Interface
311
303
305

FIG. 3

FIG. 4A

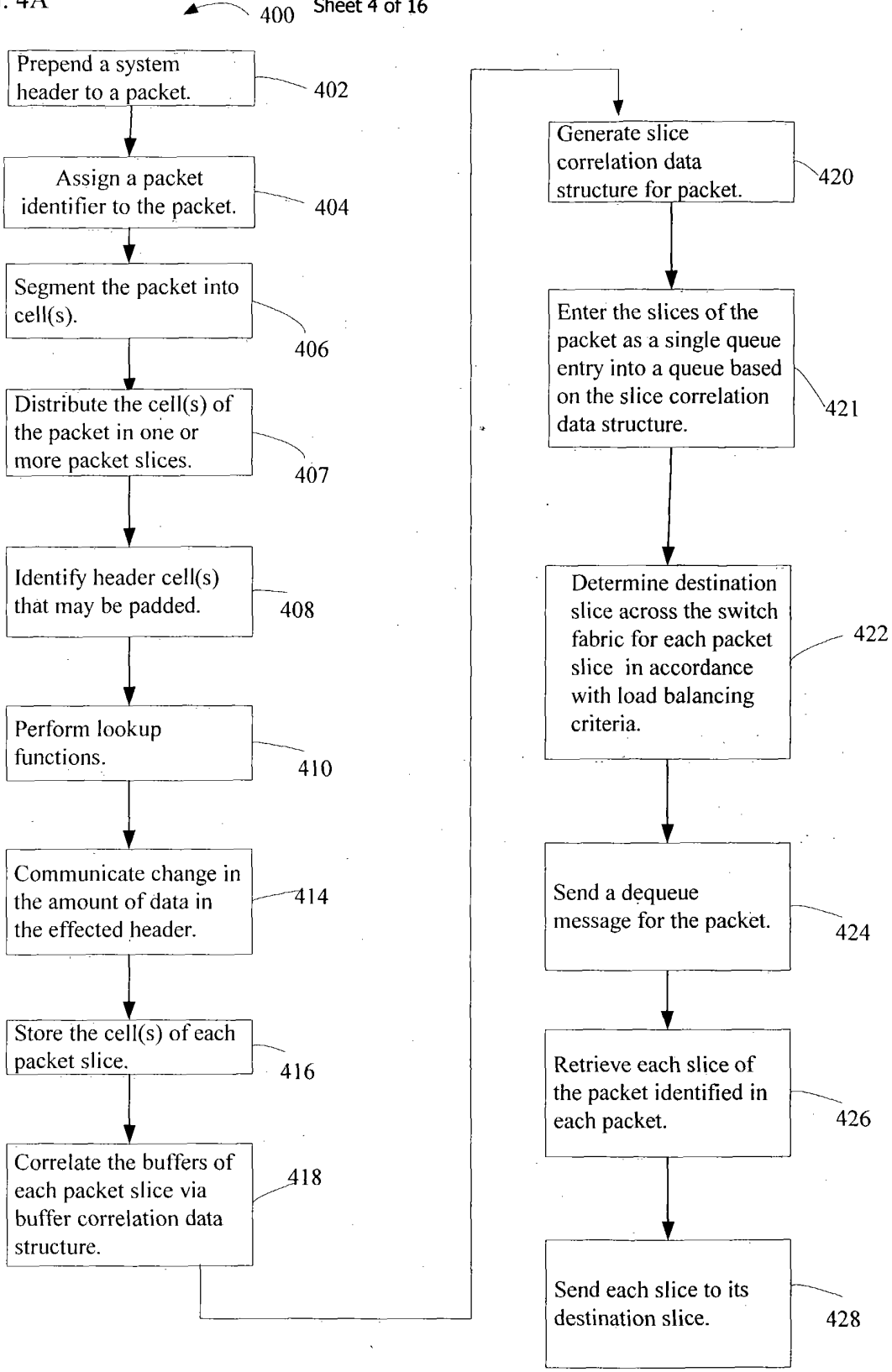
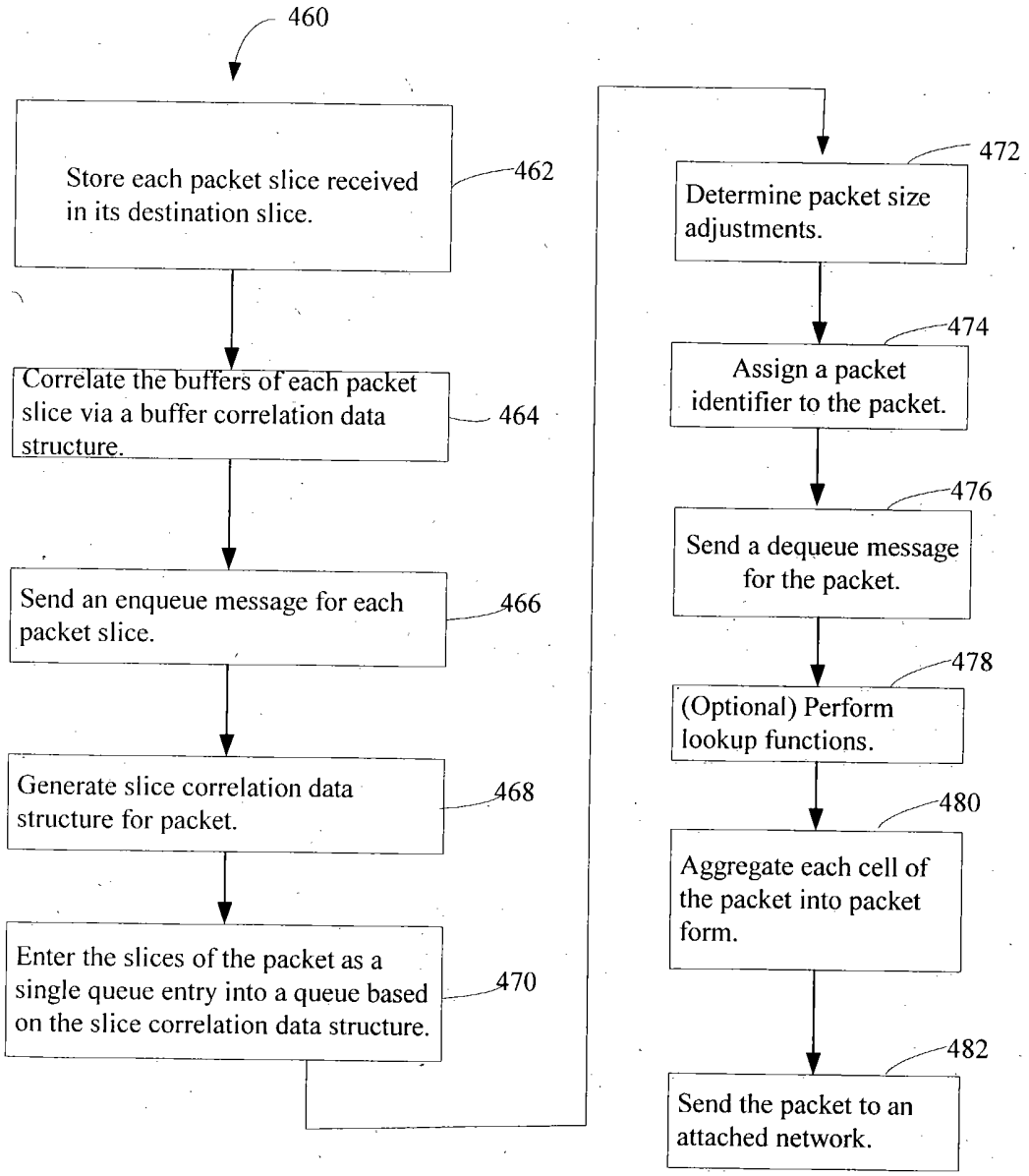
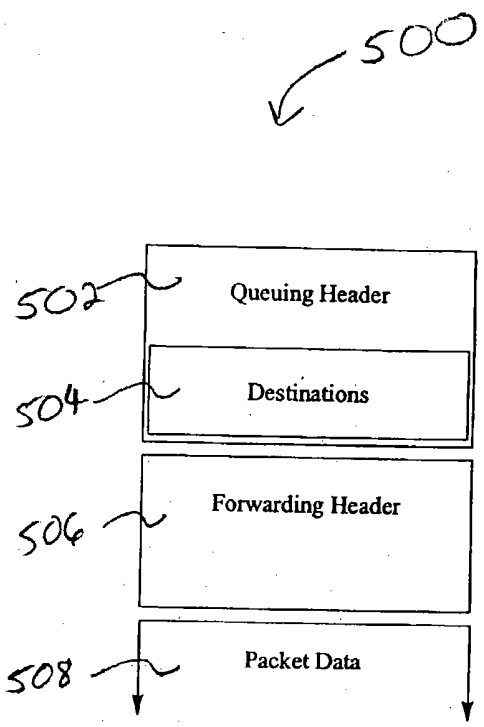
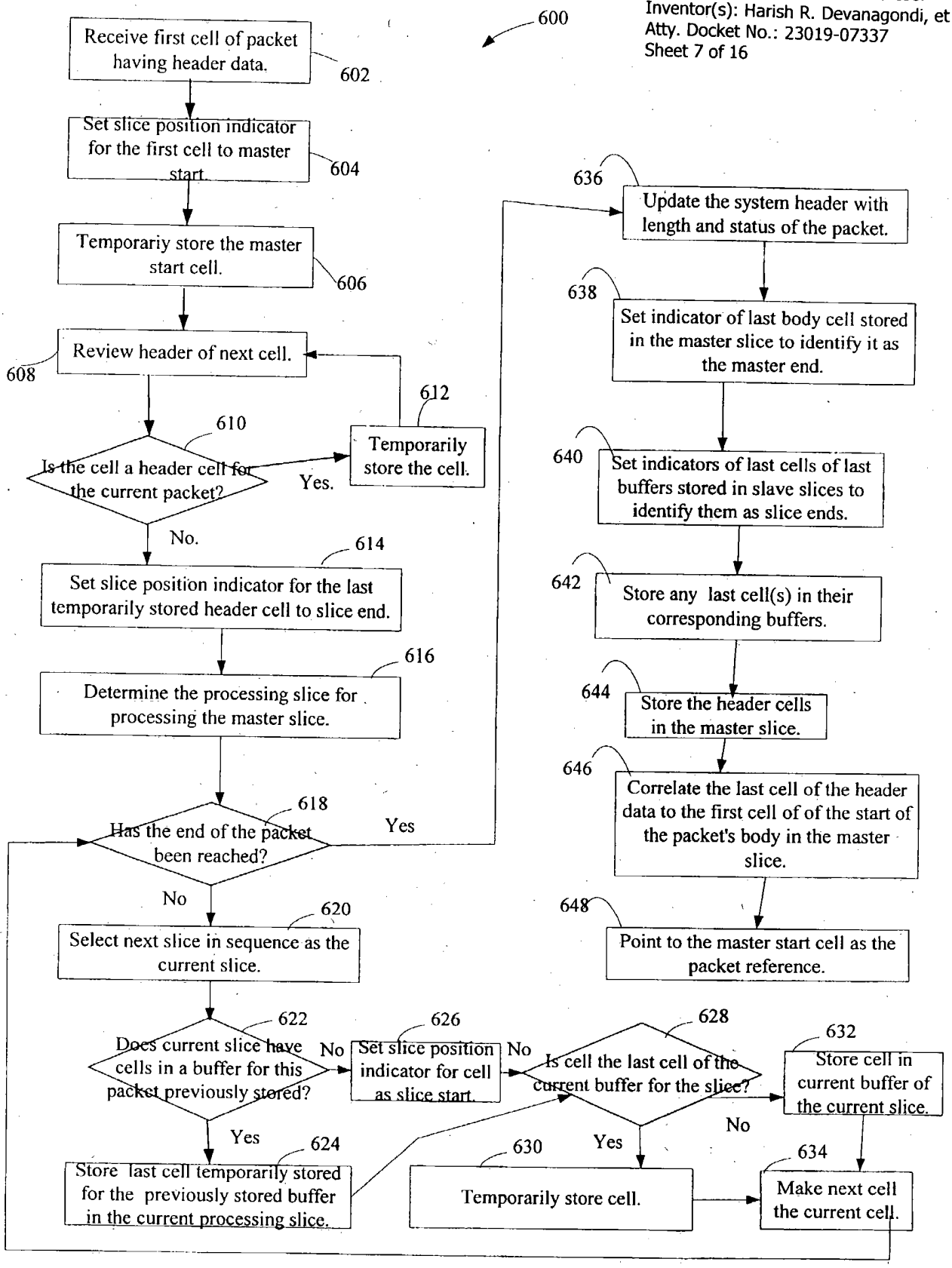

400
Prepend a system header to a packet.
402
Assign a packet identifier to the packet.
404
Segment the packet into cell(s).
406
Distribute the cell(s) of the packet in one or more packet slices.
407
Identify header cell(s) that may be padded.
408
Perform lookup functions.
410
Communicate change in the amount of data in the effected header.
414
Store the cell(s) of each packet slice.
416
Correlate the buffers of each packet slice via buffer correlation data structure.
418
Generate slice correlation data structure for packet.
420
Enter the slices of the packet as a single queue entry into a queue based on the slice correlation data structure.
421
Determine destination slice across the switch fabric for each packet slice in accordance with load balancing criteria.
422
Send a dequeue message for the packet.
424
Retrieve each slice of the packet identified in each packet.
426
Send each slice to its destination slice.
428

FIG. 4B


460
Store each packet slice received in its destination slice.
462
Correlate the buffers of each packet slice via a buffer correlation data structure.
464
Send an enqueue message for each packet slice.
466
Generate slice correlation data structure for packet.
468
Enter the slices of the packet as a single queue entry into a queue based on the slice correlation data structure.
470
Determine packet size adjustments.
472
Assign a packet identifier to the packet.
474
Send a dequeue message for the packet.
476
(Optional) Perform lookup functions.
478
Aggregate each cell of the packet into packet form.
480
Send the packet to an attached network.
482


500
502
Queuing Header
504
Destinations
506
Forwarding Header
508
Packet Data


600
Receive first cell of packet having header data.
602
Set slice position indicator for the first cell to master start.
604
Temporariy store the master start cell.
606
Review header of next cell.
608
Is the cell a header cell for the current packet?
610
Yes.
Temporarily store the cell.
612
No.
Set slice position indicator for the last temporarily stored header cell to slice end.
614
Determine the processing slice for processing the master slice.
616
Has the end of the packet been reached?
618
Yes
No
Select next slice in sequence as the current slice.
620
Does current slice have cells in a buffer for this packet previously stored?
622
No
Set slice position indicator for cell as slice start.
626
No
Is cell the last cell of the current buffer for the slice?
628
Yes
Store last cell temporarily stored for the previously stored buffer in the current processing slice.
624
Temporarily store cell.
630
No
Store cell in current buffer of the current slice.
632
Make next cell the current cell.
634
Yes
Update the system header with length and status of the packet.
636
Set indicator of last body cell stored in the master slice to identify it as the master end.
638
Set indicators of last cells of last buffers stored in slave slices to identify them as slice ends.
640
Store any last cell(s) in their corresponding buffers.
642
Store the header cells in the master slice.
644
Correlate the last cell of the header data to the first cell of of the start of the packet's body in the master slice.
646
Point to the master start cell as the packet reference.
648

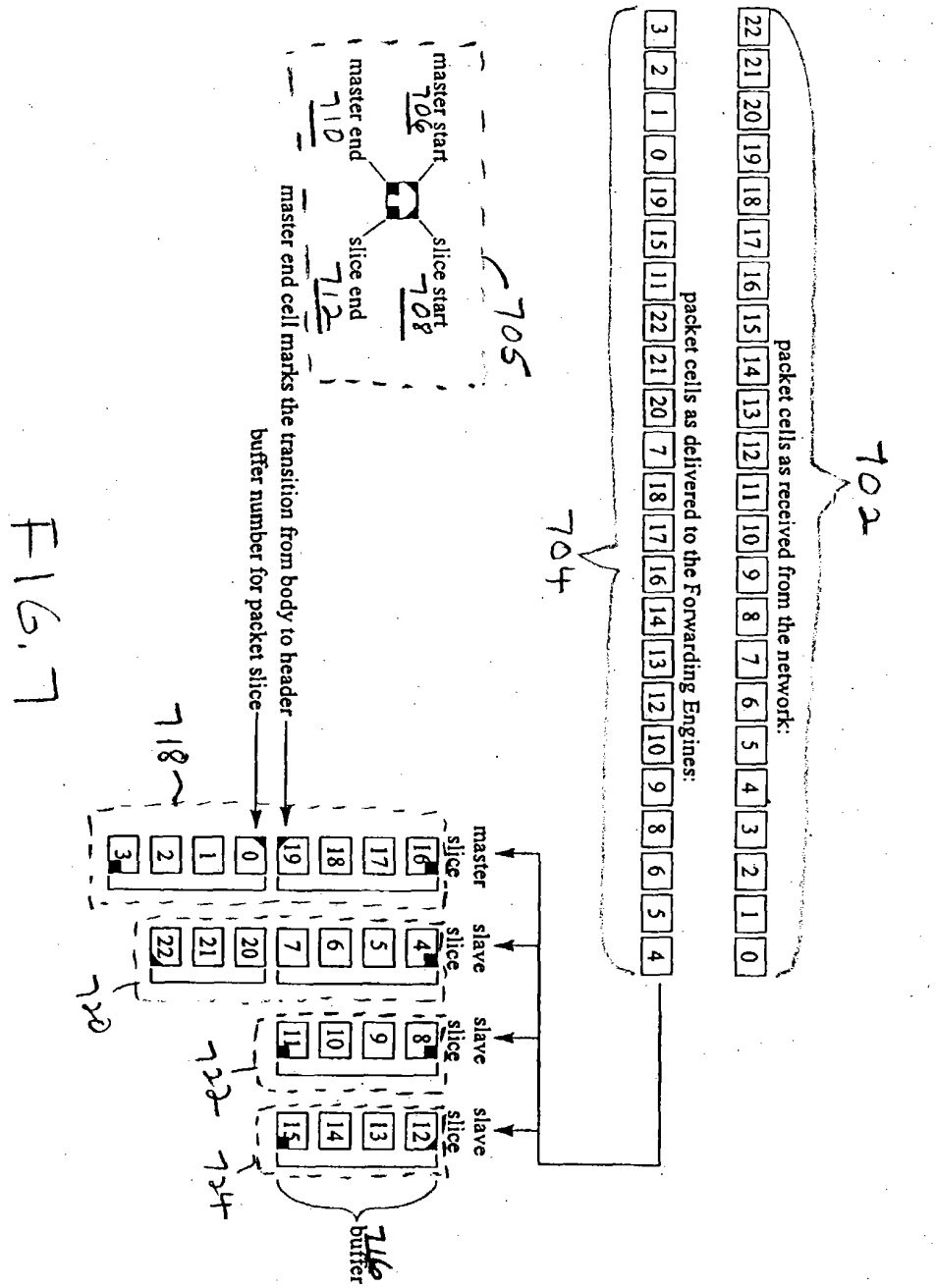
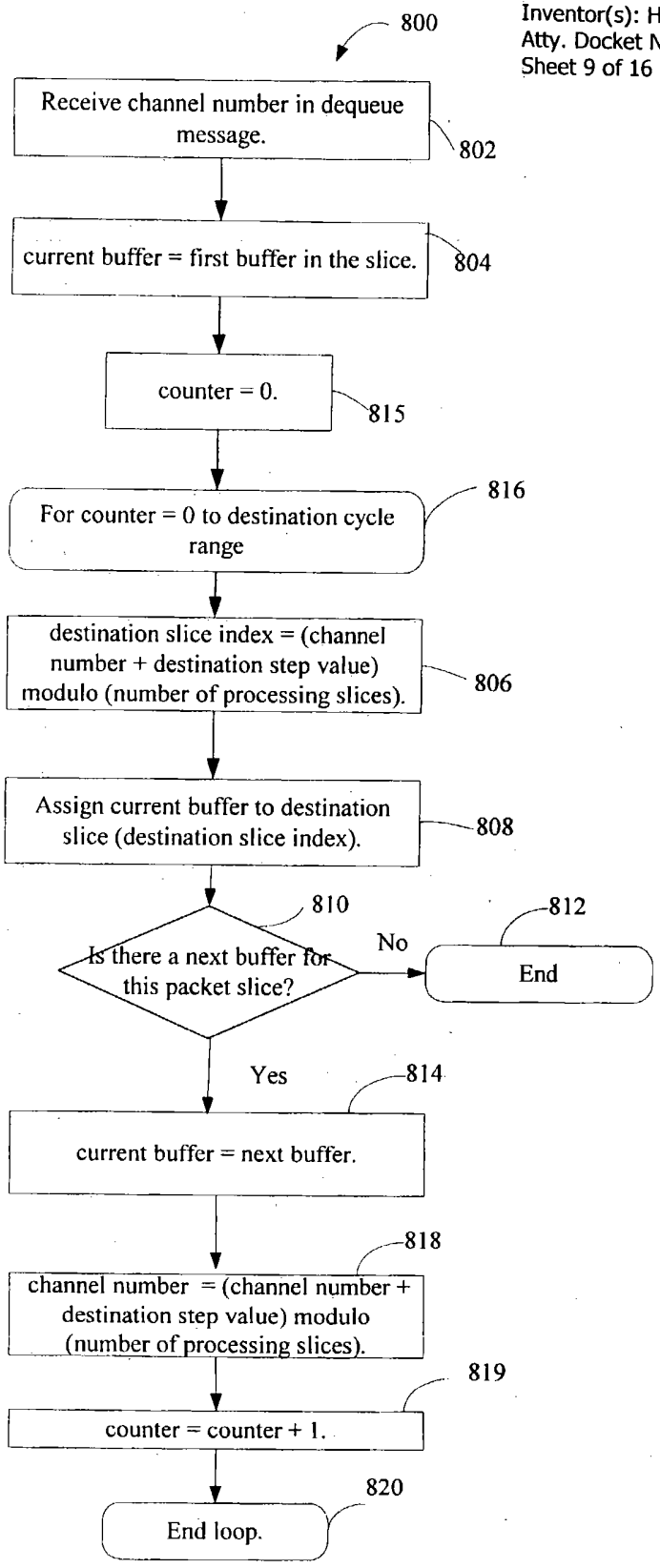

702
packet cells as received from the network:
22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
packet cells as delivered to the Forwarding Engines:
3 2 1 0 19 15 11 22 21 20 7 18 17 16 14 13 12 10 9 8 6 5 4
704
705
master start 706
slice start 708
master end 710
slice end 712
master end cell marks the transition from body to header
buffer number for packet slice
718
master slice
slave slice
slave slice
slave slice
720
722
724
buffer 716

FIG. 7

FIG. 8


800
Receive channel number in dequeue message.
802
current buffer = first buffer in the slice.
804
counter = 0.
815
For counter = 0 to destination cycle range
816
destination slice index = (channel number + destination step value) modulo (number of processing slices).
806
Assign current buffer to destination slice (destination slice index).
808
Is there a next buffer for this packet slice?
810
No
End
812
Yes
current buffer = next buffer.
814
channel number = (channel number + destination step value) modulo (number of processing slices).
818
counter = counter + 1.
819
End loop.
820

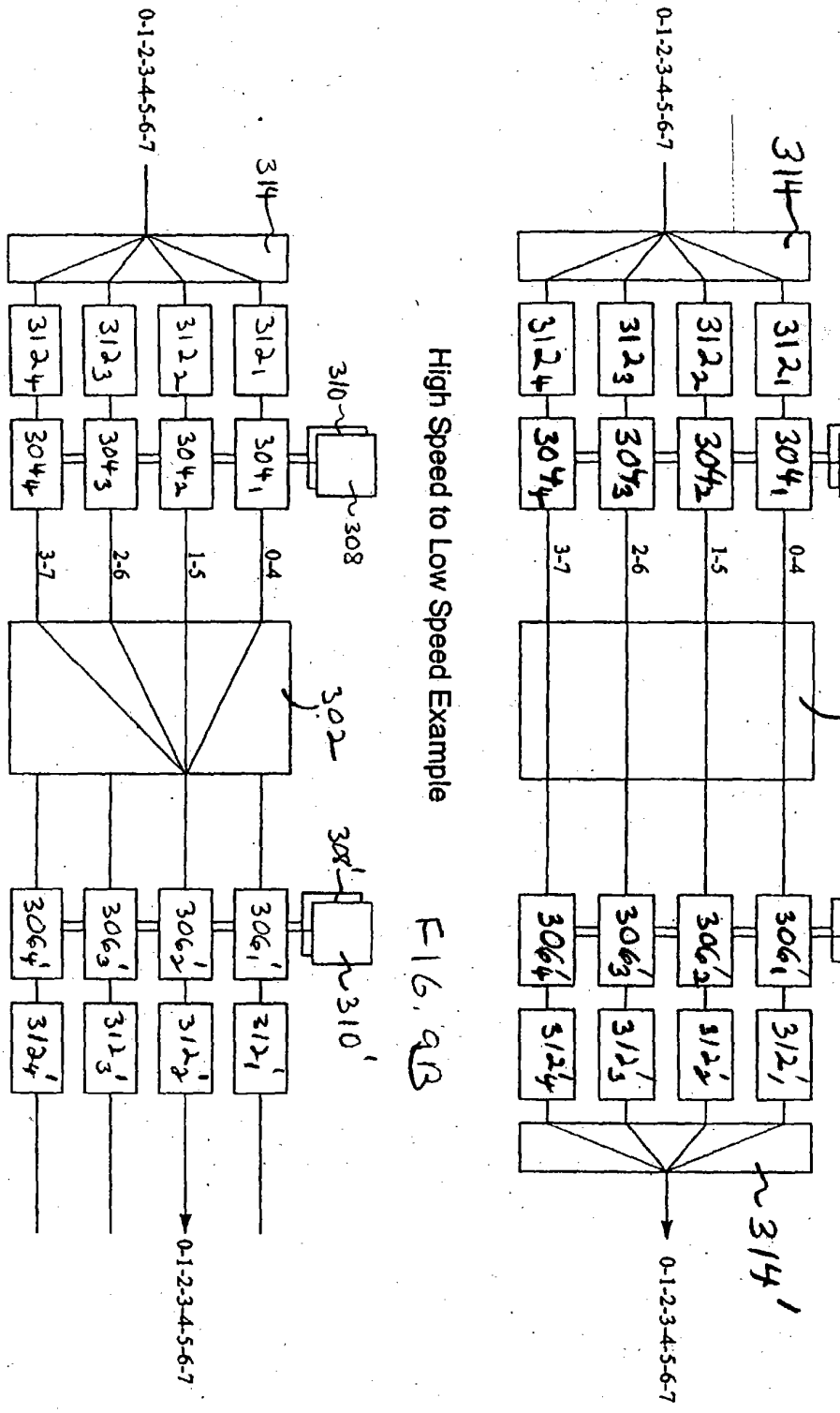
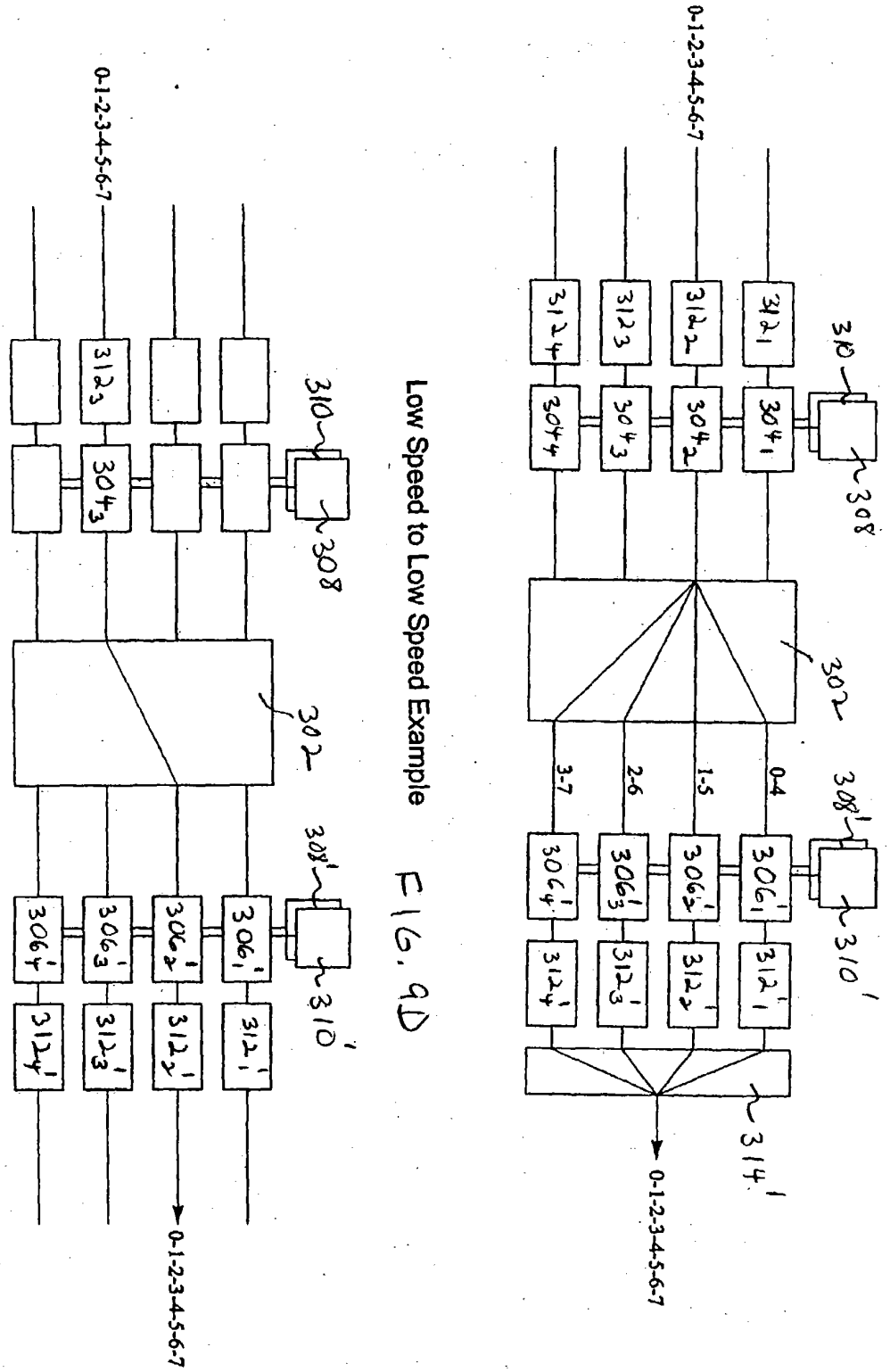

High Speed to High Speed Example
0-1-2-3-4-5-6-7
314
3121
3122
3123
3124
310
308
3041
3042
3043
3044
3-7
2-6
1-5
0-4
302
310'
308'
3061'
3062'
3063'
3064'
3121'
3122'
3123'
3124'
314'
0-1-2-3-4-5-6-7

FIG. 9A

High Speed to Low Speed Example
0-1-2-3-4-5-6-7
314
3121
3122
3123
3124
310
308
3041
3042
3043
3044
3-7
2-6
1-5
0-4
302
310'
308'
3061'
3062'
3063'
3064'
3121'
3122'
3123'
3124'
0-1-2-3-4-5-6-7

FIG. 9B


Low Speed to High Speed Example
FIG. 9C
0-1-2-3-4-5-6-7
310
308
3121
3122
3123
3124
3041
3042
3043
3044
302
3-7
2-6
1-5
0-4
308'
310'
3061'
3062'
3063'
3064'
3121'
3122'
3123'
3124'
314'
0-1-2-3-4-5-6-7
Low Speed to Low Speed Example
FIG. 9D
0-1-2-3-4-5-6-7
310
308
3123
3043
302
308'
310'
3061'
3062'
3063'
3064'
3121'
3122'
3123'
3124'
0-1-2-3-4-5-6-7

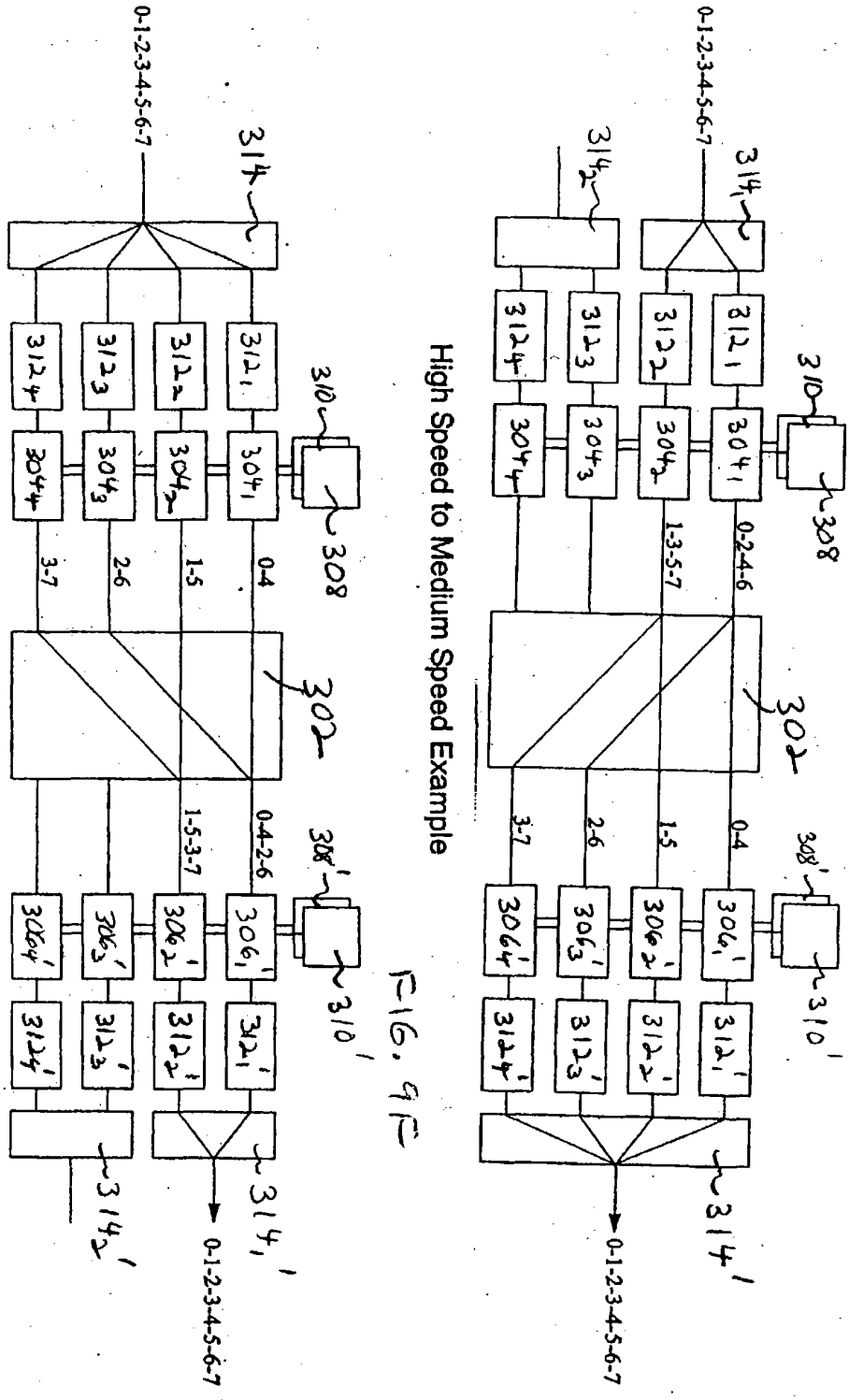

0-1-2-3-4-5-6-7
314
3121
3122
3123
3124
310
308
3041
3042
3043
3044
0-2-4-6
1-3-5-7
302
308'
310'
3041'
3042'
3043'
3044'
3121'
3122'
3123'
3124'
0-4
1-5
2-6
3-7
314'
0-1-2-3-4-5-6-7
High Speed to Medium Speed Example
Medium Speed to High Speed Example

FIG. 9E

FIG. 9F

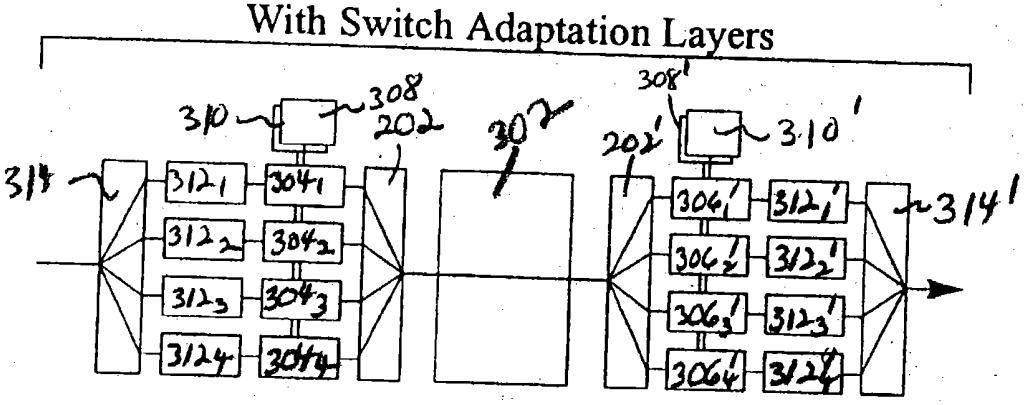

With Switch Adaptation Layers
310
308
202
302
308'
202'
310'
314
314'
312₁
312₂
312₃
312₄
304₁
304₂
304₃
304₄
306₁'
306₂'
306₃'
306₄'
312₁'
312₂'
312₃'
312₄'

FIG. 9G

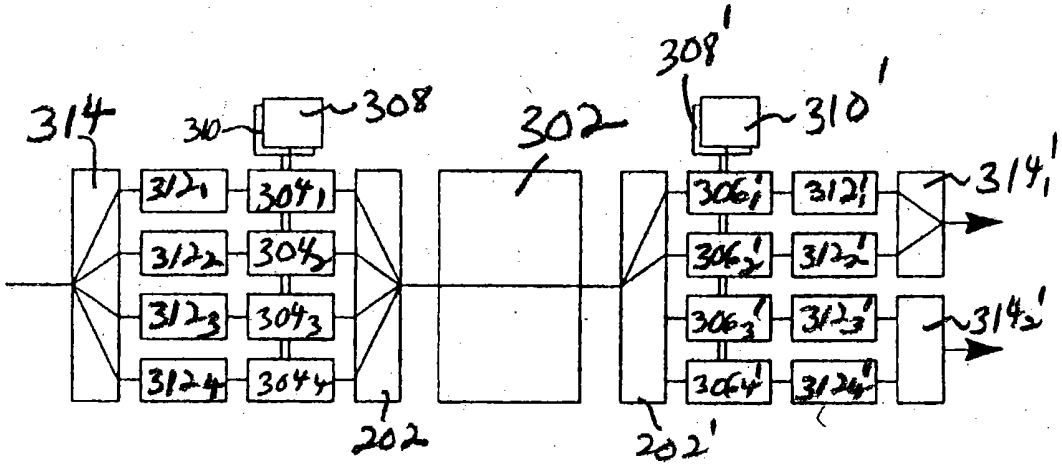

314
308
302
308'
310'
314'1
314'2
312'1
312'2
312'3
312'4
306'1
306'2
306'3
306'4
304'1
304'2
304'3
304'4
202
202'

FIG. 9H

FIG. 10A

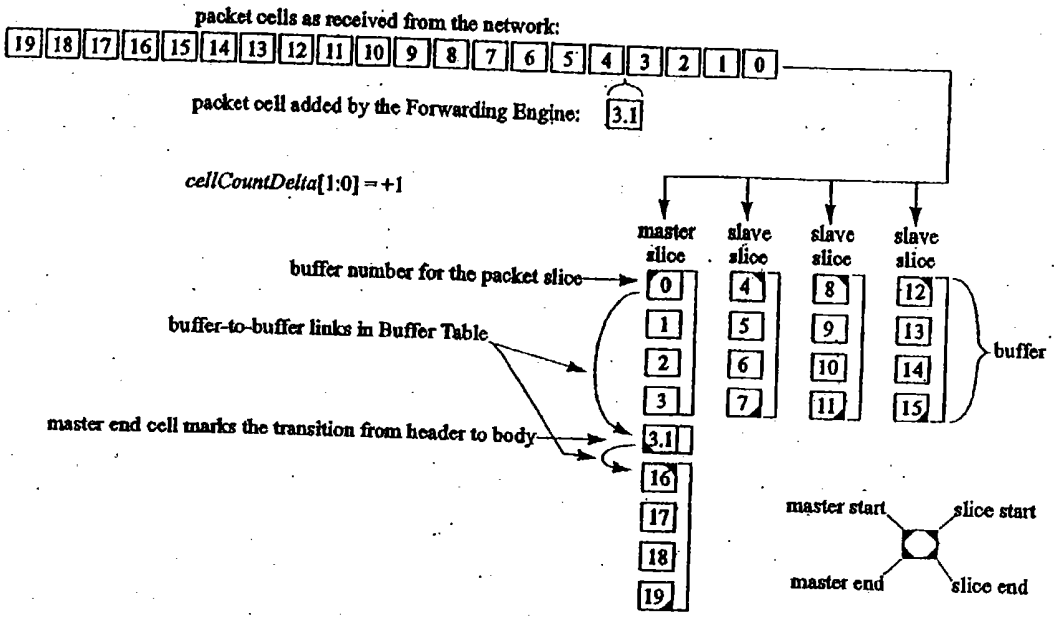


FIG. 10B

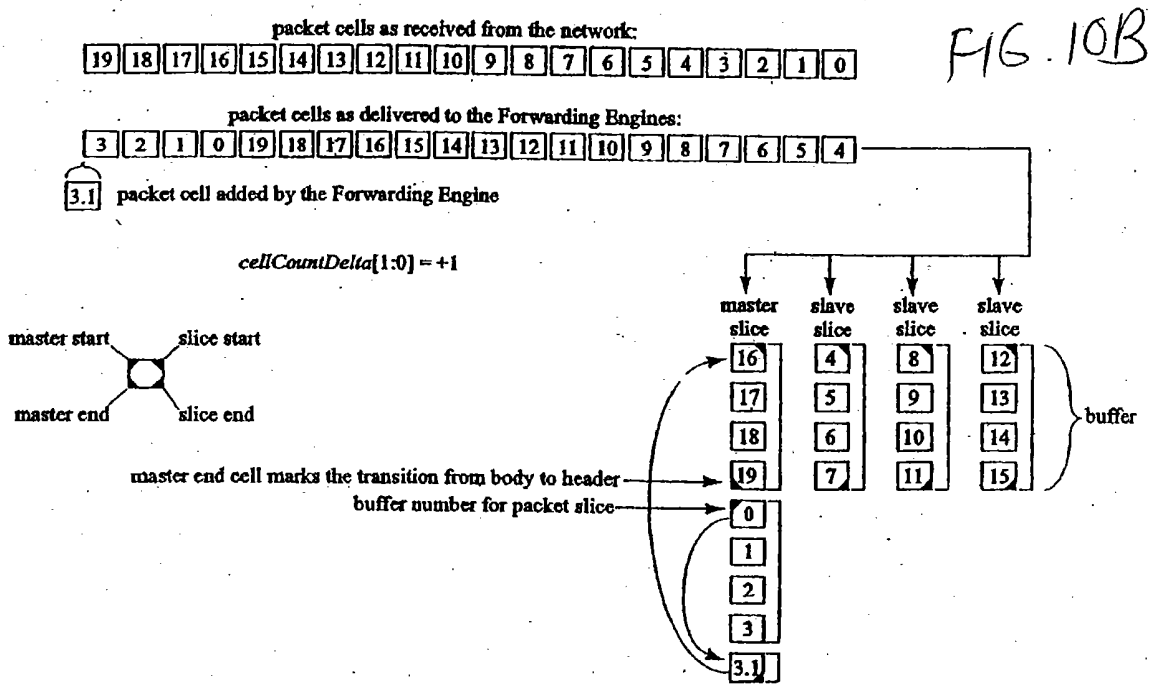


FIG. 10C

Cell Sequencing on Egress Store

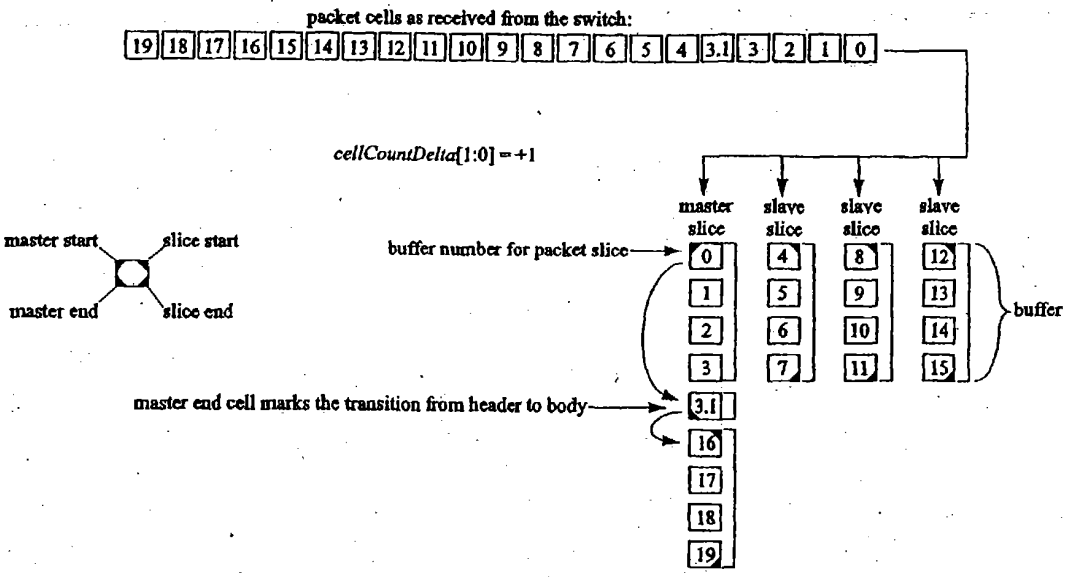
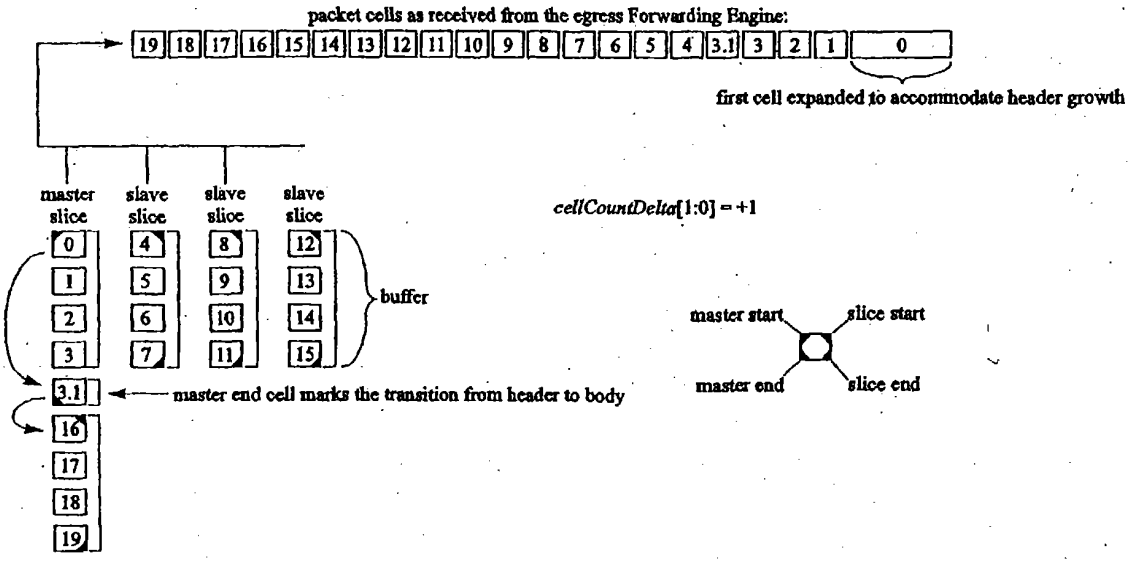


FIG. 10D

Cell Sequencing and Elasticity on Egress Retrieve